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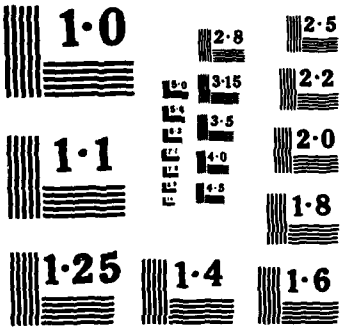

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Fault tolerance, multiprocessor, distributed data processing, software support, testbed, computer-aided design.

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

A VAX 11/780 computer was obtained to provide a software development environment for the Fault Tolerance/Distributed Computing Laboratory (FTDCL) at Auburn University. The FTDCL is a four-processing element multiprocessor, utilizing four shared memory modules and an experimental connection network to provide a testbed to evaluate fault-tolerant designs. The VAX provides a tool to develop and compile programs and an operating environment which allows programs to be loaded into the multiprocessor and experiments to be controlled and analyzed.

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HARDWARE ACQUISITION FOR THE ENHANCEMENT OF A FAULT TOLERANCE/ DISTRIBUTED COMPUTIN LABORATORY

Final Report

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August 7, 1985

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1.0 INTRODUCTION

The Fault Tolerance/ Distributed Computing Laboratory (FTDCL) at Auburn University is a facility developed under the sponsorship of the U.S. Army Ballistic Missile Defense Advanced Technology Center (BMDATC) for the purpose of conducting experiments to test and evaluate various candidate fault tolerance techniques for use in multiprocessor computer systems which may be employed for Ballistic Missile Defense (BMD). The FTDCL is unique in that it's structure can be modified as needed to support various hardware-oriented approaches to fault tolerant multiprocessor design. This cannot easily be done at other BMDATC testbeds, since the structures of these systems must remain fixed to support a variety of users on a daily basis. The FTDCL facility consists of a tightly-coupled multiprocessor, currently constructed around four single-board computers, four shareable memory modules and an experimental "shuffle/exchange" interconnection network. [1] The processors in this system work in parallel on various tasks within an overall problem, cooperating by exchanging and sharing data through the common memory. Additional keywords: distributed processing; VAX 11/780 computers; computer aided design.

The project supported by the U.S. Army Research Office under contract DAAG29-82-G-0006, entitled "Hardware Acquisition for the Enhancement of a Fault Tolerance/ Distributed Computing Laboratory", is summarized

in this report. Under this project, a flexible software support environment has been developed for the FTDCL, allowing a number of tools which were developed to support BMDATC work in the Advanced Research Center (ARC) in Huntsville to be utilized for experiment development in the FTDCL. This support environment is hosted on a VAX 11/780 computer which was obtained through the funds provided by ARO under this project, a donation from Intergraph Corporation, and additional funds provided by the Engineering Experiment Station at Auburn University. Section II of this report will describe the FTDCL software support environment, Section III will briefly describe the major development work that has taken place using this support, and section III will describe several related projects that have utilized the system purchased under this project.

II. FTDCL HARDWARE UPGRADE

A block diagram of the FTDCL system is shown in Figure 1, the main components being the four processing elements (PE's), the four shared memory modules (SM's), the interconnection network (IN), and the HOST computer - the VAX 11/780. The HOST consists of the VAX 11/780 processor, 2 Mb of memory, 900 Mb of disk storage, 48 communication ports, interactive graphics design station, and 8 pen plotter. Of the communication ports, seven are interfaced to the FTDCL - one line to each of the four PE's and one to each of the three terminals used for software development and experiment monitoring and control. The remaining ports on the VAX support various other users in the

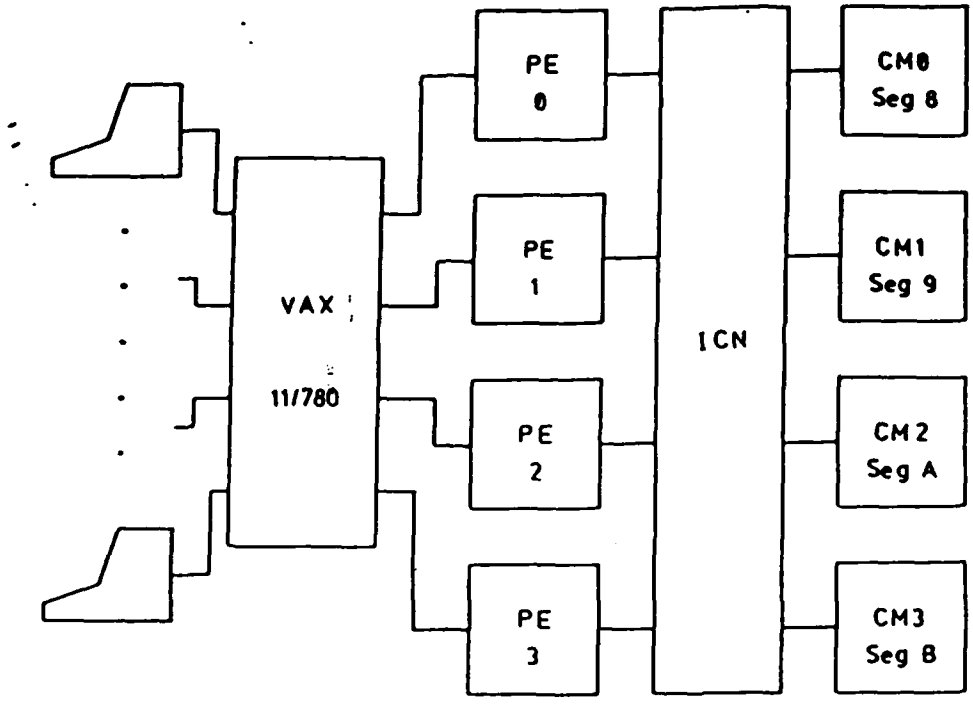

Figure 1. Hardware Configuration of the FTDCL

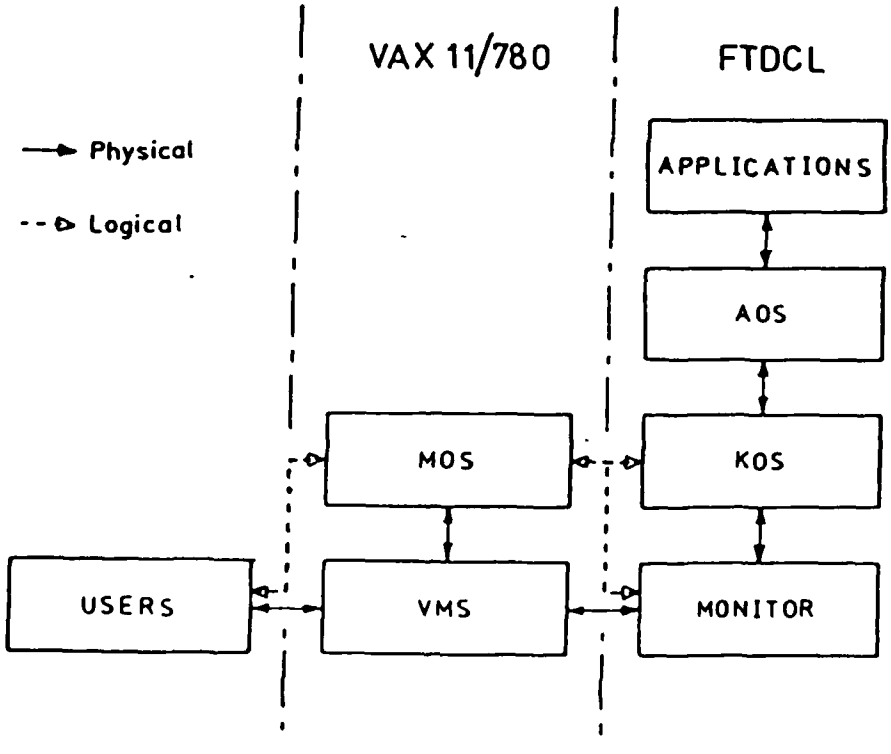

Figure 2. Software Configuration of the FTDCL

Electrical Engineering Department at Auburn.

All software for the FTDCL multiprocessor is entered and compiled on the HOST, after which the compiled object code is down-loaded into one or more PE's via their serial communication lines. In addition to the standard VAX text editors, the other software support tools utilized in this process are the Process Design Language (PDL) compiler provided by the BMD ARC [2], the Microbench Z8000 Assembler, and a variety of library management and linking tools from the ARC and Microbench, as well as a number of tools developed at Auburn. Once code has been compiled into one or more object modules, a program on the HOST called the "Master Operating System" (MOS) is used to allow a user to interface with the FTDCL multiprocessor via a menu of commands. These commands allow the user to download the object code to one or more PE's in the multiprocessor, run and interact with the experiment, receive results, and store information into files for later analysis. The operation of the MOS program is more fully described in [3].

On the FTDCL multiprocessor itself is a three layer operating system, as shown in Figure 2. The Z8000 monitor was adapted from a monitor program supplied by Zilog with the original Z8000 processor single board computers used in the FTDCL. The monitor provides a number of communication facilities and software debugging facilities on the

board. The Kernel Operating System (KOS), described in [3], provides the run-time support for PDL programs running on each individual processor. It allows processes to be scheduled and executed, memory space to be allocated and deallocated, and communications to take place between multiple processes on the system. In addition, it passes information to the MOS on the HOST to provide experiment feedback, as well as receiving information from the HOST for experiment control. The KOS is downloaded from the HOST to each PE prior to the downloading of any application programs into the system. The third operating system layer is the Global Operating System (GOS), described in [4], which provides overall control of the multiprocessor. The GOS is responsible for scheduling processes to be assigned to PE's, maintaining a list of available global memory, coordinating interprocess communication, and maintaining a number of error detection and recovery features. Error detection performed by the GOS includes diagnosis of IN and SM faults, maintenance of a system-wide clock in conjunction with monitoring process deadlines, and other features. The GOS has been made flexible enough to support different scheduling strategies and different hardware configurations so that a variety of experiments can be performed.

Currently in the FTDCL, experiments are in progress which will be examining the operation of a fault tolerant SM module and various fault tolerance approaches to the IN design. These experiments should provide useful information in the design and developement of BMD data processing systems in the near future.

III. RELATED WORK

The VAX 11/780 system purchased under this project has provided support for a number of other activities related to Department of Defense research activities at Auburn, in addition to the software support of the FTDCL as described above. This section of the report will discuss briefly the nature of some of these related activities.

Computer-aided design (CAD) is extremely critical in the development of large and very large scale integrated circuit (VLSI) devices. The Intergraph VAX 11/780 system with its interactive design station has been used to develop a number of CAD tools for VLSI development, ranging from schematic capture to system and circuit simulation at various levels of detail, chip layout for mask generation, design rule checking, etc. The first of these tools, a chip layout program, was used in the development and fabrication of a mask for an LSI chip which implements a switch to be used in the interconnection network of the FTDCL, described above and in [1,5]. This chip, when fabricated and tested, will allow a significant reduction in the components of the FTDCL, and will facilitate the expansion of the system and the incorporation of redundancy in the connection network of the system for fault tolerance.

CAD tools are also critical for the study and evaluation of new computer architectures for defense and aerospace systems. Several

projects at Auburn, sponsored by the U.S. Army Missile Command, the Missile Intelligence Agency, and NASA, are utilizing the VAX 11/780 for such study and evaluation. Activities range from simulation of systems and components with various hardware description languages, to the development of expert systems for use in defense applications. More recently, work has begun in the study of power systems for space-based defense systems at Auburn University's Space Power Institute. The VAX 11/780 described above will be used for a variety activities in this critical study.

IV. SUMMARY

The hardware purchased with funds from this project has significantly upgraded the capabilities of the Fault Tolerance/ Distributed Computing Laboratory at Auburn University, supporting studies involving fault tolerance and reliability of data processing systems for BMD applications. The VAX 11/780 has provided a unique software development environment to support experiments on the FTDCL multiprocessor system. These studies have and will continue to provide insights to BMDATC regarding techniques for the design of ultrareliable systems, identifying the various cost, performance, and reliability tradeoffs of candidate fault tolerant design techniques as they apply to BMD applications.

In addition to support of the FTDCL, the VAX 11/780 has become a vital tool in a variety of other projects sponsored by various U.S. Army and other government agencies, providing support for CAD activities,

system simulation, analysis, and in general providing a powerful computation tool. In the future, this system will continue to provide support to these and other defense related projects, allowing the Electrical Engineering Department at Auburn to maintain the high standards it has set for its research activities.

V. REFERENCES

1. Nelson, V.P., et al, "Fault Tolerance and Architectural Reliability in Distributed Data Processing Systems - Part I - Testbeds for BMD-DDP Applications", Tech. Rep. AU-EE-84-0011-1, Auburn University, July 24, 1984.

2. Vosbury, N. and McDonald, B., "PDL User's Manual", Tech. Rep. TM-HU-306/000/00, System Development Corporation, 15 May, 1981.

3. Brooks, D.A., "A Kernel Operating System for the Fault Tolerant Multiprocessor Laboratory", M.S. Thesis, Auburn University, Dec. 1984.

4. Chutigusol, S. "An Operating System for a Multiprocessor", M.S. Thesis, Auburn University, Aug. 1985.

5. Hsu, Y.J., Nelson, V.P., and R.C, Jaeger, "A Gate-Array Design of a Shuffle/Exchange Network Switching Element", Proc. Sixth Biennial University/ Government/ Industry Microelectronics Symposium, Auburn, Alabama, June 1985, pp. 158-164.

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